What is claimed is:

[Claim 1] 1. A switched capacitor circuit comprising:

an operational amplifier having a first input terminal and a first output terminal;

a first sampling capacitor having a first terminal and a second terminal, the first terminal being connected to the first input terminal of the operational amplifier;

a first signal input switch controlled by a first clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the first sampling capacitor, the second terminal being used for receiving a first input signal;

a first reference input switch controlled by a second clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the first sampling capacitor, the second terminal being used for receiving a first reference signal;

a first input reset switch controlled by a third clock having a first terminal and a second terminal, the first terminal being connected to the first input terminal of the operational amplifier, the second terminal being used for receiving a common signal;

a first reference reset switch controlled by a reset clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the first reference input switch, the second terminal being used for receiving the common signal; and

a first feedback network connected between the first input terminal of the operational amplifier and the first output terminal of the operational amplifier.

[Claim 2] 2. The switched capacitor circuit of claim 1, further comprising:

a reference signal circuit for generating the first reference signal and the common signal.

[Claim 3] 3. The switched capacitor circuit of claim 1, further comprising:

a clock generator for generating the first clock, the second clock, the third clock, and the reset clock, wherein a phase change of the first clock, a phase change of the second clock,

and a phase change of the reset clock do not occur at the same time.

[Claim 4] 4. The switched capacitor circuit of claim 1, wherein the first feedback network comprises:

a first feedback capacitor having a first terminal and a second terminal, the first terminal being connected to the first input terminal of the operational amplifier;

a first input feedback switch controlled by the first clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the first feedback capacitor, the second terminal being used for receiving the first input signal; and

a first output feedback switch controlled by the first clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the first feedback capacitor, the second terminal being connected to the first output terminal of the operational amplifier.

[Claim 5] 5. The switched capacitor circuit of claim 1, wherein the operational amplifier further comprises a second input terminal and a second output terminal, the first input terminal and the second input terminal are a differential input pair of the operational amplifier, the first output terminal and the second output terminal are a differential output pair of the operational amplifier, and the switched capacitor circuit further comprises:

a second sampling capacitor having a first terminal and a second terminal, the first terminal being connected to the first input terminal of the operational amplifier;

a second signal input switch controlled by the first clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the first sampling capacitor, the second terminal being used for receiving a second input signal;

a second reference input switch controlled by the second clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the first sampling capacitor, the second terminal being used for receiving a second reference signal;

a second input reset switch controlled by the third clock having a first terminal connected to the first input terminal

of the operational amplifier and a second terminal for inputting the common signal;

a second reference reset switch controlled by the reset clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the first reference input switch, the second terminal being used for receiving the common signal; and

a second feedback network connected between the second input terminal and second output terminal of the operational amplifier.

[Claim 6] 6. The switched capacitor circuit of claim 5, further comprising:

a reference signal circuit for generating the first reference signal, the second reference signal, and the common signal.

[Claim 7] 7. The switched capacitor circuit of claim 5, wherein the second feedback network comprises:

a second feedback capacitor having a first terminal and a second terminal, the first terminal being connected to the second input terminal of the operational amplifier;

a second input feedback switch controlled by the first clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the second feedback capacitor, the second terminal being used for receiving the second input signal; and

a second output feedback switch controlled by the first clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the second feedback capacitor, the second terminal being connected to the second output terminal of the operational amplifier.

[Claim 8] 8. An analog to digital converter comprising:

a clock generator for generating a first clock, a second clock, a third clock, and a reset clock, wherein a phase change of the first clock, a phase change of the second clock, , and a phase change of the reset clock do not occur at the same time;

a reference signal circuit for generating a first reference signal, a second reference signal, and a common signal; and

a plurality of switched capacitor circuits connected in series and connected between an analog input terminal and a digital

output terminal, each of the switched capacitor circuits comprising:

an operational amplifier having a first input terminal and a first output terminal;

a first sampling capacitor having a first terminal and a second terminal, the first terminal being connected to the first input terminal of the operational amplifier;

a first signal input switch controlled by a first clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the first sampling capacitor, the second terminal being used for receiving a first input signal;

a first reference input switch controlled by a second clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the first sampling capacitor, the second terminal being used for receiving a first reference signal;

a first input reset switch controlled by a third clock having a first terminal and a second terminal, the first terminal being connected to the first input terminal of the operational amplifier, the second terminal being used for receiving a common signal;

a first reference reset switch controlled by a reset clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the first reference input switch, the second terminal being used for receiving the common signal; and

a first feedback network connected between the first input terminal and the first output terminal of the operational amplifier,

wherein a first input terminal of an operational amplifier within each of the switched capacitor circuits connected in series is connected to a second terminal of a first signal input switch of a next switched capacitor circuit of the switched capacitor circuits connected in series, a second input terminal of a first signal input switch within a first of the switched capacitor circuits connected in series is connected to the analog input terminal, and a first output terminal of an operational amplifier within a last of the switched capacitor circuits connected in series is connected to the digital output terminal.

[Claim 9] 9. The analog to digital converter of claim 8, wherein the operational amplifier of each of the switched capacitor circuits further comprises a second input terminal and a second output terminal, the first

input terminal of the operational amplifier and the second input terminal of the operational amplifier are a differential input pair of the operational amplifier, the first output terminal of the operational amplifier and second output terminal of the operational amplifier are a differential output pair, and each of the switched capacitor circuits further comprises:

a second sampling capacitor having a first terminal and a second terminal, the first terminal being connected to the first input terminal of the operational amplifier;

a second signal input switch controlled by the first clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the first sampling capacitor, the second terminal being used for receiving a second input signal;

a second reference input switch controlled by the second clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the first sampling capacitor, the second terminal being used for receiving a second reference signal;

a second input reset switch controlled by the third clock having a first terminal and a second terminal, the first terminal being connected to the first input terminal of the operational amplifier, the second terminal being used for receiving the common signal;

a second reference reset switch controlled by the reset clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the first reference input switch, the second terminal being used for receiving the common signal; and

a second feedback network connected between the second input terminal of the operational amplifier and second output terminal of the operational amplifier.

[Claim 10] 10. The analog to digital converter of claim 8, wherein the first feedback network comprises:

a first feedback capacitor having a first terminal and a second terminal, the first terminal being connected to the first input terminal of the operational amplifier;

a first input feedback switch controlled by the first clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the first

feedback capacitor, the second terminal being used for receiving the first input signal; and

a first output feedback switch controlled by the first clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the first feedback capacitor, the second terminal being connected to the first output terminal of the operational amplifier.

[Claim 11] 11. The analog to digital converter of claim 9, wherein the second feedback network comprises:

a second feedback capacitor having a first terminal and a second terminal, the first terminal being connected to the second input terminal of the operational amplifier;

a second input feedback switch controlled by the first clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the second feedback capacitor, the second terminal being used for receiving the second input signal; and

a second output feedback switch controlled by the first clock having a first terminal and a second terminal, the first terminal being connected to the second terminal of the second feedback capacitor, the second terminal being connected to the second output terminal of the operational amplifier.

[Claim 12] 12. A method of operating a switched capacitor circuit, the switched capacitor circuit comprising an operational amplifier, a first sampling capacitor, a first signal input switch, a first reference input switch, a first reference reset switch, and a first feedback network, the method comprising:

after turning off the first reference input switch, turning on the first signal input switch to transmit a first input signal to the first sampling capacitor and turning on the first reference switch to transmit a common signal to a second terminal of the first reference input switch;

turning off the first reference reset switch, and then turning off the first signal input switch; and

turning on the first reference input switch after turning off the first signal input switch.

[Claim 13] 13. The method of claim 12, wherein the first feedback network comprises a first feedback capacitor, a first input feedback switch, and a first output feedback switch, the method further comprising:

turning on the first input feedback switch when turning on the first signal input switch; and
turning on the first reference input switch when turning on the first output feedback switch.

[Claim 14] 14. The method of claim 12, wherein the operational amplifier further comprises a second input terminal and a second output terminal, the first input terminal of the operational amplifier and the second input terminal of the operational amplifier are a differential input pair of the operational amplifier, the first output terminal of the operational amplifier and the second output terminal of the operational amplifier are a differential output pair of the operational amplifier, the switched capacitor circuit further comprises a second sampling capacitor, a second signal input switch, a second reference input switch, a second reference reset switch and a second feedback network, and the method further comprises:

turning on the second signal input switch when turning on the first signal input switch;
turning on the second reference input switch when turning on the first reference input switch; and
turning on the second reference reset switch when turning on the first reference reset switch.

[Claim 15] 15. The method of claim 14, wherein the second feedback network comprises a second feedback capacitor, a second input feedback switch, and a second output feedback switch, and the method further comprises:

turning on the second input feedback switch when turning on the first signal input switch; and
turning on the second output feedback switch when turning on the first reference input switch.